AMENDMENTS

In the Written Description

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

Please substitute the following annotated paragraph for the paragraph beginning on p. 9, line 15:

Simultaneously, while an instruction held in a thread control element is prohibited to execute during a cycle due to one or more source operands matching one or more temporary registers in the temporary register ID/thread control ID pipelines, the arbiter may allow the execution of a second instruction held in a second thread control element to proceed in that cycle provided that none of the source operands of the second instruction matches any of the temporary registers in the temporary register ID/thread control ID pipelines. For example, if at least one of the source operands of the instruction held in TC0 matches at least one of the temporary registers in the temporary register ID/thread control ID pipelines in a cycle, the arbiter may allow an instruction held in TC1 to proceed in that cycle provided that none of the source operands of the instruction held in TC1 matches any of the temporary registers in the temporary register ID/thread control ID pipelines. In a further example, in a cycle, if both instructions held in TC0 and TC1 have at least one source operand each that match one or more temporary registers in the pipelines, the arbiter may then allow a third instruction held in TC2 to proceed in that cycle provided that none of the source operands of the instruction held

in TC2 matches any of the temporary registers in the temporary register ID/thread control ID pipelines. If all the ~~instruction~~ instructions held in the thread control elements have at least one source operand matching a temporary register in the pipelines in that cycle, the arbiter does not grant any of the instruction requests in that cycle and will only grant an instruction request when at least one of the thread control elements holds an instruction whose source operands do not match any of the temporary registers in the temporary register ID/thread control ID pipelines.